Final Exam

- 10:30am, May 16th
- Close book; close notes
- Use the provided cheat sheets, available on the course home page, as is.
- Also bring a copy of the Figure 2.25
- Comprehensive; roughly 80% after midterm
- If you want special arrangements (IN, etc.), present your request before the final.

Course Grade

- Before I submit your grade, you will be informed via email
  - your final exam mark,
  - your entire record of the semester,
  - my equations of calculating course grades, and
  - your course grade.
Lecture 2: MIPS ISA

You are expected to
- Know common MIPS instructions
- Know instruction formats
- Be able to translate assembly instructions to their machine instruction counterparts and vice versa
- Program short assembly codes

Lecture 3: Programming in MIPS

- NOT covered

Lecture 4: IA32

- NOT covered
Lecture 5 ALU

- You are expected to understand
  - Signed and unsigned numbers
  - Signed arithmetic, overflows
  - Supporting logic instructions
  - Supporting SLT and subtraction
  - Put them together
  - Carry look-ahead adder
  - multiplication

Lecture 6: Single Cycle Datapath

- NOT covered

Lecture 7: Multi Cycle Datapath

- NOT covered

Lecture 8: Floating Point

- NOT covered
Lecture 9: YH16

You are expected to

- Program in YH16 ISA
- Understand how instructions are accomplished cycle by cycle.
- To be able to design the control logic that carries out these cycles/steps.
- Understand the state transition diagram

- Design digital circuits for all modules in the datapath.
- Be familiar with the data flows of all instructions on the datapath, cycle by cycle.
- Give control signal values to execute instructions, cycle by cycle.
- Give boolean expressions for all control signals
- Give cycle by cycle execution of new instructions.
Lecture 10: Performance

You are expected to
- Understand the three factors in computer performance
- Compute CPI, execution time, MIPS
- Be familiar with Amdahl's Law
- Understand the tradeoff between clock rate and CPI, and their relationship with datapath

Lecture 11: Cache

You are expected to understand
- the concepts of locality
- Associativities
- The purposes of address bits
- Replacement policies, write handling strategies, …

- Circuits NOT covered
Lectures 12: Pipelining

You are expected to

- Understand the concept
- Be familiar with the 5 MIPS pipeline stages.
- Understand the three pipeline hazards and their solutions

Consider the code below and answer the following

- (15pt) Point out instances of ALU forwarding.
- (10pt) Point out instances of memory forwarding.
- (25pt) Starting with the instruction pipeline empty, calculate the number of cycles to execute the MIPS code. The count starts with the first cycle of `add` to the fifth cycle of `slt`.

```
add r2,r4,r3
lw  r5,0(r2)
sw  r10,4(r2)
beq r5, r2, A
sub r12,r4,r3
or  r30,r15,r16
A: xor r20,r12,r13
slt r3,r30,r32
```

```
Consider the code below running on a 2MHz pipelined MIPS Lite. The loop iterates 1000 times.

- (15pt) Compute CPI.
- (10pt) Compute MIPS.
- (15pt) 10% of the memory references cause cache misses. A cache miss takes extra 12 cycles to access the main memory. Compute CPI again.

```
loop: lw r4, 0(r1)
      addi r1, r1, 4
      lw r5, 0(r2)
      addi r2, r2, 4
      add r6, r4, r6
      sw r6, 0(r3)
      addi r7, r7, 1
      bne r7, r8, loop
      addi r3, r3, 4
```