CS 465 – Computer Systems Architecture (Summer 2025)
Department of Computer Science
George Mason University

COURSE INFORMATION

Course Number and Title:	CS 465 – Computer Systems Architecture
Section Number and CRN:	Section B01 – CRN 43038
Class Duration:	May 27, 2025, to July 26, 2025 (Summer Session B: 8 weeks)
Class Meeting Time:	Online Asynchronous
Class Location:	Canvas

***Important Notice*:** This is an online asynchronous class. Students are required to view and listen to video lectures on Canvas, complete online assessments on Canvas, log on to GMU VPN to access Zeus, and download, print, type, draw, scan, and upload files, from/to Canvas and Gradescope.

GENERAL INFORMATION

Instructor:	Angkul Kongmunvattana, Ph.D. (Dr. K)
E-mail address:	akongmun@gmu.edu (start your "Subject" line with [CS465])
Office Location:	ENGR 4428, Fairfax Campus
Office Hours:	By appointments only (must be scheduled via GMU email at least 24 hours in advance)

TEXT AND RESOURCES

Recommended Textbooks:

- David Patterson and John Hennessy, *Computer Organization and Design (MIPS Edition): The Hardware/Software Interface*, Fifth Edition, MKP, 2014.
- John Hennessy and David Patterson, *Computer Architecture: A Quantitative Approach*, Fifth Edition, MKP, 2012.

COURSE CATALOG DESCRIPTION

Computer subsystems and instruction set architectures. Single-cycle, multiple-cycle, and pipeline architectures. Memory hierarchy, cache memory, and virtual memory input-output processing. Offered by Computer Science. Limited to two attempts.

Credit hours: 3
Prerequisite: CS 367 with a grade of C or higher.

COURSE OUTCOMES

- Students will be able to analyze and compare performance characteristics of a computer.
- Students will be able to demonstrate knowledge of instruction set architectures; be able to show how instructions are represented at both the machine level and in the context of a symbolic assembler; be able to read and write small assembly programs.
- Students will be able to manipulate low-level data representations and understand the implementation of computer arithmetic operations.
- Students will be able to explain how an instruction is executed; be able to explain the role of data path and control; be able to explain pipelining and the relevant improvement technologies.
- Students will be able to understand the effect and implementation of memory hierarchy, in particular, the role of cache and virtual memory.
- Students will become familiar with advanced topics and the latest evolvement in computer architecture.

TOPICS

Digital Logic Circuit Analysis and Design
Computer Arithmetic
Computer Organization and Design
Instruction Set Architecture (Accumulator, Stack, GPR, and CISC vs RISC, etc.)
Instruction Level Parallelism (Pipelining, Data and Control Hazards, Data Forwarding Techniques, VLIW, Superscalar, Out-of-order Execution, Scoreboard, Tomasulo, and Branch Prediction Techniques, etc.)
Thread Level Parallelism (SMT, CMP, etc.)
Memory Hierarchy (Registers, Cache, RAM, VM, SSD, and HDD, etc.)
Cache Organization
Cache Write Policies (Write-Through, Write-Back, Write-Once, and Write Allocate, etc.)
Cache Coherence Protocols
Memory Consistency Models
Interconnection Networks
Contemporary Issues in Computer Architecture

EVALUATION METHODS

Exercises	5%
Quizzes	20%
Assignments	15%
Midterm Exam	20%
Final Exam	40%

COURSE GRADING

Grade	Cut-Off	Grade	Cut-Off	Grade	Cut-Off	Grade	Cut-Off
A+	98%	B+	88%	C+	78%	D	60%
A	92%	B	82%	C	72%	F	0%
A-	90%	B-	80%	C-	70%		

COURSE CONTENT AND CALENDAR (tentative)

Session	Video Lectures Release Date	Topic
1	May 27	Class Administration and Overview
2	May 28	Digital Logic Circuit Analysis and Design (1)
3	May 29	Digital Logic Circuit Analysis and Design (2)
4	June 03	Computer Arithmetic
5	June 04	Computer Organization and Design
6	June 05	Instruction Set Architecture
7	June 10	ILP (1)
8	June 11	ILP (2)
9	June 12	ILP (3)
10	June 17	TLP
11	June 18	Memory Hierarchy
12	June 19	Midterm Review
Midterm Exam	June 23 to 29	Midterm Exam (up to and include ILP)
13	July 1	Cache Organization
14	July 2	Cache Write Policies

15	July 3	Cache Coherence Protocols (1)
16	July 8	Cache Coherence Protocols (2)
17	July 9	Cache Coherence Protocols (3)
18	July 10	Memory Consistency Models
19	July 15	Interconnection Networks
20	July 16	Contemporary Issues in Computer Architecture
21	July 17	Final Review
Final Exam	July 21 to 26	Final Examination (Cumulative)

COURSE POLICIES

Exercise Policy

Exercises are given on Canvas, covering materials in each topic. Exercises are designed to check and to reinforce the learning of materials. Exercises can be taken multiple times. A score from the highest attempt will be recorded. Exercises cannot be completed after the last day of class (07/26/2025).

Quiz Policy

Quizzes are also given on Canvas and can be attempted only once. There are no make-up quizzes. A quiz is assigned when substantial topics have been covered in class and practiced through exercises. Each quiz is 30 to 60 minutes in duration, depending on the complexity of the topics. When assigned, quizzes are released at 6:00pm on Monday with a due date at 6pm on Sunday of the same week. While quizzes will remain open after their due dates for studies and reviews, late quizzes will get a zero grade. A grade of zero will be assigned for the missed quiz without an excused absence (e.g., illness, unforeseen emergency, etc.). If the instructor deems the absence is excused, then the final exam grade will also be used for the missed quiz.

Assignment Policy

Assignments are also given on Canvas and submitted via Canvas to Gradescope. They are assigned when substantial topics have been covered in class, practiced through exercises, and preliminary assessed through quizzes. When assigned, assignments are released at 6pm on Monday with a due date at 6pm on Sunday of the same week. No late submissions will be accepted. Students are expected to type their work (NOTE: Handwritten answers can also be scanned, but any illegible and/or ambiguous answers will be treated as if they do not exist) and submit it as a PDF file. A grade of zero will be assigned for the missed assignment without an excused absence (e.g., illness, unforeseen emergency, etc.). If the instructor deems the absence is excused, then the final exam grade will also be used for the missed assignment.

Midterm Exam Policy

Midterm exam is an open-book, open-note online exam via Canvas. It is scheduled for the week of June 23rd, 2025, to June 29th, 2025. It can only be taken once during that week. Once started, students will have 90 minutes to complete and submit their answers. A grade of zero will be assigned for the missed midterm exam without an excused absence (e.g., illness, unforeseen emergency, etc.). If the instructor deems the absence is excused, then the final exam grade will also be used for the missed midterm exam.

Final Exam Policy

Final exam is also an open-book, open-note online exam via Canvas. It covers all materials. It is scheduled for the week of July 21st, 2025, to July 26th, 2025. It can only be taken once during that week. Once started, students will have 2 hours and 30 minutes to complete and submit

their answers. According to the University Policy (AP.3.10.1), absences from final exam will not be excused by the instructor (except for sickness).

Grade Contesting Policy
You have one week after grades are released to contact the instructor with a grading issue. After this one-week period, no grades will be changed.

There are no extra-credit assignments and/or projects.

COURSE POLICY ADDENDUM

Students are expected to refer to the Common Course Policies for the following information. Students will be held responsible for knowing this information.

- Academic Standards
- Accommodation for Students with Disabilities
- FERPA and Use of GMU Email Addresses for Course Communication
- Title IX Resources and Required Reporting

IMPORTANT DATES

Midterm Exam	June 23 to 29, 2025 (90 minutes online)
Final Exam	July 21 to 26, 2025 (150 minutes online)

See Summer 2025 Academic Calendar for other important dates.

The syllabus may be adjusted if deemed necessary by the instructor.